REMARKS

After entry of this amendment, claims 1-2, 8-11, 13-14, 17-18, and 20-37 are pending. In the present Office Action, claims 1-19 were rejected under 35 U.S.C. § 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992 ("Killian"). Claims 6-12, 16, and 19 were rejected under 35 U.S.C. § 112, second paragraph. Applicants respectfully traverse these rejections and request reconsideration. Claims 3 and 15 were objected to. However, since claims 3 and 15 have been cancelled, Applicants submit that the objection is moot.

Claims 1-2, 8-11, 13-14, and 17-18

Applicants respectfully submit that each of claims 1-2, 8-11, 13-14, and 17-18 recites a combination of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "said execution core is configured to zero extend said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number".

Applicants can find no teaching or suggestion in Killian for the above highlighted combination of features. Particularly, Applicants can find no teaching or suggestion in Killian to "preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits". Applicants note the Office Action's analysis with regard to claim 6 (Office Action, page 5, item 16). However, this analysis relies on the register being a source of an instruction. Claim 1 clearly recites that the register is a destination of the instruction, and an execution core configured to "preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits". Applicants submit that the operation of a processor on a source register does not apply to the combination of features recited in claim 1.

For at least the above stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 2 and 8-11, being dependent from claim 1, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 2 and 8-11 recites additional combinations of features not taught or suggested in the cited art.

Claim 13 recites a combination of features including: "zero extending said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits; and preserving a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number." The teachings of Killian, highlighted above, do not teach or suggest the above highlighted combination of features of claim 13. Accordingly, Applicants submit that claim 13 is patentable over the cited art. Claims 14 and 17-18, being dependent from claim 13, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 14 and 17-18 recites additional combinations of features not taught or suggested in the cited art.

New Claims 20-37

Applicants respectfully submit that each of new claims 20-37 recite combinations of features not taught or suggested in the cited art. For example, claim 20 recites a combination of features including: "said execution core is configured to zero extend said result for update in said storage location responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution circuit is configured to preserve a value of at least a portion of said bits in said storage location that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number". Claims 21-25 depend from claim 20, and recite additional combinations of features not taught or suggested in the cited art.

Claim 26 recites a combination of features including "said execution core is configured to extend said result to said first number of bits for update in said storage location responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution circuit is configured to preserve a value of at least a portion of said bits in said storage location that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number". The cited art does not appear to teach or suggest the above highlighted combination of features. Claims 27-31 depend from claim 26 and recite additional combinations of features not taught or suggested in the cited art.

Claim 32 recites a combination of features including "said execution core is configured to zero extend said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number". The cited art does not appear to teach or suggest the above highlighted combination of features. Claims 33-34 depend from claim 32 and recite additional combinations of features not taught or suggested in the cited art.

Claim 35 recites a combination of features including "said execution core is configured to extend said result to said first number of bits for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number". The cited art does not appear to teach or suggest the above highlighted combination of features. Claims 36-37 depend from claim 35 and recite additional combinations of features not taught or suggested in the cited art.

Section 112 Rejection

The section 112 rejection allegedly rejects claims 6-12, 16, and 19. However, rejections are only specified for claims 6, 9, 11, 12, 16, and 19. Claims 6, 12, 16, and 19 have been cancelled, and thus rejections of these claims are moot.

Claim 9 has been amended to recite "an encoding of said instruction" in place of "said instruction's encoding". Claim 11, being dependent from claim 9, recites "said encoding". Applicants submit that the amendments address the section 112 rejection of claims 9 and 11.

Objection to Declaration

The Office Action objected to the declaration as defective for stating that a provisional priority claim was not applicable when there is a priority claim to provisional application serial no. 60/224,368. The Office Action referred to MPEP 602.01 and 602.02 in the objection. Applicants submit that nothing in MPEP 602.01 and 602.02 requires that the declaration identify a priority claim to a provisional application. Rather, MPEP 602 requires that FOREIGN priority claims be included in the declaration (or in an application data sheet), but is silent on the issue of priority claims to provisional patent applications. Applicants are aware of no requirement to include the priority claim to a provisional application in the declaration, even if the declaration includes a space to insert such a claim. Applicants also note that the current declaration form provided by the Office (PTO/SB/01) includes a section for foreign priority claims, but no section for provisional application priority.

Accordingly, Applicants submit that the declaration is not defective and furthermore that priority to the provisional application is properly claimed in the present application.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-64000/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

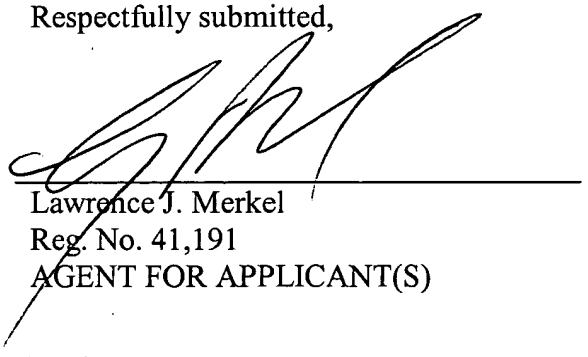
☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☒ Please charge the above-identified deposit account in the amount of $402 for fees ($258 for three excess independent claims and $144 for 8 excess claims over 20).

☒ Other: IDS

Respectfully submitted,



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